

# Suspending superconducting qubits by silicon micromachining

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We present a method for relieving aluminum 3D transmon qubits from a silicon substrate using micromachining. Our technique is a high yield, one-step deep reactive ion etch that requires no additional fabrication processes, and results in the suspension of the junction area and edges of the aluminum film. The drastic change in the device geometry affects both the dielectric and flux noise environment experienced by the qubit. In particular, the participation ratios of various dielectric interfaces are significantly modified, and suspended qubits exhibited longer  $T_1$ 's than non-suspended ones. We also find that suspension increases the flux noise experienced by tunable SQUID-based qubits.

The coherence times of superconducting qubits have steadily increased over the past decade due to careful engineering of the electromagnetic environment, better materials and fabrication methods, and improved device designs that minimize loss. State-of-the-art superconducting qubits with the longest lifetimes ( $T_1$ ) make use of very low loss tangent dielectric substrates and have large separation between planar conductors to decrease the effect of dielectric loss in the interfaces between materials<sup>1-3</sup>. In particular, it has been shown that for aluminum 3D transmons on sapphire,  $T_1$  times are limited by the various interfaces between the dielectric substrate, the superconducting metal, and vacuum<sup>4</sup>. This effect can be attributed to the larger electric fields near metallic surfaces and the higher concentration of two-level systems (TLS) at disordered interfaces<sup>5-7</sup>. At the same time, magnetic impurities at the surface of superconductors have been proposed as the cause of  $1/f$  flux noise that limits the performance of SQUID based qubits and sensors<sup>8-10</sup>.

In order to better understand these effects, one strategy is to drastically alter the geometry of materials and interfaces that contribute to qubit loss and decoherence. In this Letter, we present a procedure for removing the substrate and suspending aluminum Josephson junctions on silicon by micromachining. Silicon is a low-loss dielectric that offers several advantages for implementing the next generation of complex quantum circuits<sup>11,12</sup>. Its prevalent use in the semiconductor and MEMS industries have led to a large variety of fabrication techniques that are not available for sapphire<sup>13</sup>. Using silicon as a substrate material enables the development of novel devices and architectures in circuit QED, such as multilayer quantum circuits that incorporate micromachined superconducting enclosures and resonators<sup>14,15</sup>. Substrate micromachining has also been used to reduce dielectric loss and frequency noise in niobium titanium nitride coplanar waveguide resonators on silicon<sup>16,17</sup>. On the other hand, silicon has a more complex surface chemistry than sapphire; for example, it forms an amorphous oxide layer

that may be host to a large number of TLS's and paramagnetic impurities<sup>11,18,19</sup>.

We suspend our qubits with a simple, one-step deep reactive ion etch (DRIE) using the BOSCH process that does not require any additional steps to mask or protect the devices<sup>16,20,21</sup>. We begin with high resistivity (100) silicon wafers ( $\rho > 10^4 \Omega\cdot\text{cm}$ ) and fabricate aluminum 3D transmon qubits using the standard Dolan bridge double-angle deposition technique<sup>22</sup>. DRIE is then performed directly on the fabricated qubits. This is possible because aluminum itself is an excellent mask for the BOSCH process. We have performed this process on more than one hundred devices of various geometries, and found that the Josephson junctions were almost all unaffected except for a slight increase in the normal state resistance, possibly due to increased diffusion of the junction oxide when the devices are heated by the etching process.

Figure 1 shows a schematic drawing and scanning electron micrographs (SEM) of suspended 3D transmons. We note that all regions  $\sim 700$  nm from the edge are undercut, resulting in the junction region and the narrow  $1 \mu\text{m}$  wide leads on either side becoming completely suspended. This means that our process is compatible with aluminum based devices of any geometry, as long as suspended metal regions are supported by other larger features. The suspended single junction transmons are robust against solvent cleaning, drying, and repeated thermal cycles. We observe, however, that more complex suspended structures such as SQUID loops are more easily damaged, for example by surface tension during solvent cleaning or wet etches.

We first study the effect our process has on dielectric loss and qubit  $T_1$ . Following the analysis in Wang *et al.*<sup>4</sup>, we quantify the loss due to various dielectric materials using their participation ratios and loss tangents ( $\tan\delta$ ). In Figure 2, we plot the measured  $T_1$ 's of several types of qubits with different designs and fabrication procedures against the simulated participation ratios of their metal-substrate (MS) interfaces. Similar plots of  $T_1$  versus the substrate-air (SA) and metal-air (MA) participation ratios can be found in the supplementary materials<sup>21</sup>. In addition to qubits of the design shown in Figure 1 (Design A), we also fabricated a set of qubit designs with

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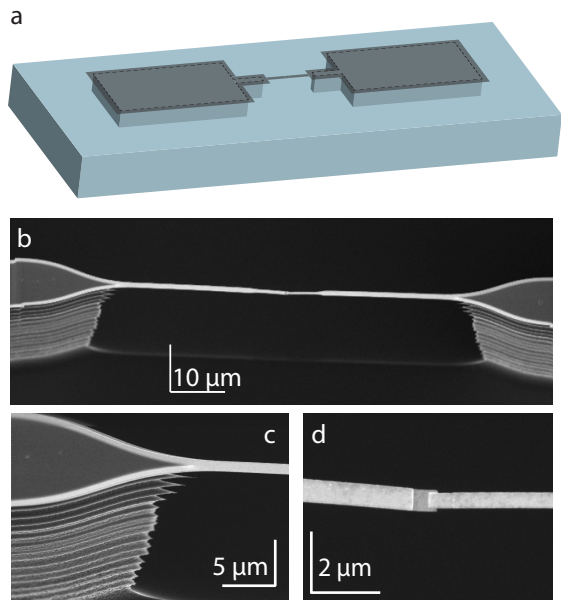


FIG. 1. **Micromachined 3D transmons using DRIE** (a) A schematic drawing of a suspended 3D transmon on silicon. An overhang is created at the edges of the metal, while thin features are suspended. (b) SEM image of a BOSCH etched transmon showing the entire suspended leads around the junction region (c) Detailed view of the supporting silicon pedestals, showing the lighter-colored overhanging Al edges and corrugated BOSCH profile. (e) Detailed view of the completely suspended Al-AIO<sub>x</sub>-Al Josephson junction.

higher surface participation (Designs B and C). Design C qubits have planar capacitors whose gaps can be varied to change the surface participations. Drawings of all qubit designs can be found in the supplementary materials<sup>21</sup>. The dielectric participation ratios were obtained through electromagnetic simulations that faithfully modeled the device geometries, including the undercut at the edge of suspended devices<sup>4,21</sup>.

Without any kind of surface preparation before or after aluminum deposition, the typical  $T_1$ 's of the Design A qubits are only a few microseconds, which is more than an order of magnitude worse than the same design on sapphire. The use of surface treatment techniques such as buffered oxide etch (BOE) or oxygen plasma ashing (OPA)<sup>21,23</sup> improves the lifetimes of the regular non-suspended qubits. DRIE further improves the  $T_1$ 's of the Design A qubits. The highest  $T_1$  measured with this procedure was  $\sim 63 \mu\text{s}$  for an etch depth of  $60 \mu\text{m}$ , which is comparable to the  $T_1$ 's of typical qubits of the same design on sapphire. We note that the qubit loss is likely frequency dependent because of coupling to resonant loss channels such as TLS's. This can lead to low  $T_1$ 's in exceptional cases, which we have also included in Figure 2. We will explore this further in our later discussion of flux tunable qubits.

The results in Figure 2 indicate that the quality of interfaces of qubits on silicon are highly dependent on sur-

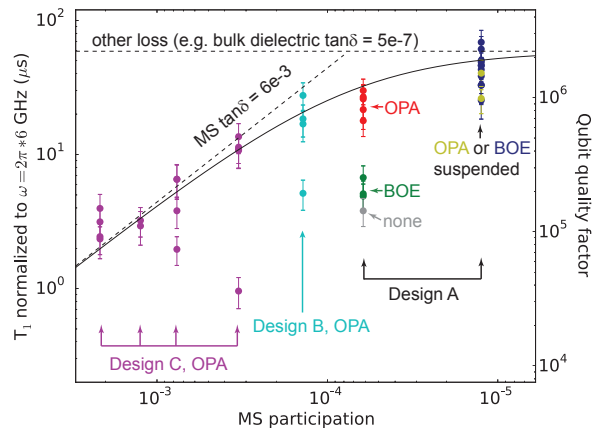


FIG. 2. **Lifetime of silicon transmons vs. metal-substrate participation ratio** Each point corresponds to one measured qubit. The MS participation of design C qubits were varied by changing planar capacitor gap distance<sup>21</sup>. The label OPA signifies oxygen plasma ashed before and after deposition, while BOE signifies buffered oxide etch before deposition only. Errorbars are typical variation of  $T_1$ 's over time. Dashed lines are guides to the eye corresponding MS surface loss and other effects that are independent of MS participation, such as bulk dielectric loss. Solid line indicates the combination of these loss mechanisms.

face treatments and are generally higher loss than those on sapphire. The  $T_1$ 's of non-suspended Design A qubits suggest that surface treatment before and after deposition is important on silicon. On the other hand, only OPA before deposition is needed to obtain  $>50 \mu\text{s}$   $T_1$ 's on sapphire<sup>4</sup>. It is possible that, for example, the liftoff process leaves more resist residue on silicon than on sapphire. In addition, any exposed silicon surface will form an oxide even after cleaning. Both resist and oxide are likely to result in a higher loss SA interface, which has comparable participation ratios as the MS interface for non-suspended qubits. This may explain the observation that while qubit  $T_1$ 's are better after surface cleaning, they never reach the levels measured on sapphire.

It is also evident from Figure 2 that it is insufficient to consider a simple model where qubit loss is dominated by single dielectric interface. The qubits with high MS participation (Design C) have  $T_1$ 's that follow a line of constant MS  $\tan\delta = 6 \times 10^{-3}$ , consistent with being limited by loss due to that interface. However, qubits with lower MS participation (Designs A and B) deviate from that line. One simple explanation for this trend is that the bulk dielectric loss for our silicon substrates becomes significant once the MS participation has been sufficiently reduced. The bulk dielectric participations of the measured qubits, including the suspended ones, are all similar to within 10%. Therefore, we can indicate the  $T_1$  limit due to bulk dielectric loss as a horizontal line in Figure 2. We find that taking into account both bulk and MS surface loss mechanisms results in a model that is consis-

tent with data from both the suspended qubits and the regular qubits that underwent OPA.

We emphasize, however, that other loss mechanisms can play a role as well. For example, the SA and MA participations scale similarly to the MS participation for the regular, non-suspended qubits<sup>4</sup>. However, unlike a change in qubit geometry, the DRIE process affects the three interfaces differently. In particular, it increases both the SA and MA participations<sup>21</sup>. Therefore, increased loss from the SA and MA interfaces could contribute to negating the  $T_1$  improvement expected from the reduced MS participation. We also cannot rule out more complex effects of the DRIE, such as a change in the SA and MA  $\tan\delta$ 's from damage or polymer deposition on these surfaces. Clearly, more investigations are needed to isolate and understand these different effects. Our results indicate that micromachining is a new technique to alter the loss contributions of various materials in ways not possible with changes in geometry alone. This can help us gain information about the roles of individual interfaces in limiting qubit  $T_1$ 's.

In order to investigate the effects of DRIE on qubit behavior in more detail, we also measured frequency dependence of the  $T_1$  and flux noise of regular and suspended tunable SQUID qubits. The qubit design is exactly the same as in Figure 1, except the single junction is replaced by a  $10\ \mu\text{m} \times 10\ \mu\text{m}$  SQUID loop, which is completely suspended after etching. A side-view SEM of a suspended SQUID transmon is shown in Figure 3a. We compare this device with another that underwent BOE before deposition and no other surface cleaning or etching after deposition. The two qubits were symmetrically arranged inside the same copper cavity to ensure that they experienced a similar background electromagnetic environment. Two separate solenoid coils mounted outside the cavity and aligned with the location of the qubits allowed us to individually control the frequency of each device.

We plot  $T_1$  as a function of qubit frequency for one pair of regular and suspended qubits in Figure 3b and 3c, respectively. For the regular qubit, we find that, in addition to a low overall  $T_1$  of  $<10\ \mu\text{s}$ , there are sharp dips in the  $T_1$  at a multitude of distinct frequencies. The suspended qubit shows a higher overall  $T_1$ , but also exhibits a few resonant features where the  $T_1$  is drastically reduced. A second pair of qubits measured in the same manner exhibited similar behavior. These observations imply that both types of qubits are affected by the presence of resonant loss channels such as TLS's, as was observed in many previous studies<sup>5,24</sup>. We observe that resonant loss channels are less prevalent for the suspended qubit than the regular qubit. However, their presence may explain the variability that we observe in the  $T_1$  measurements of single junction qubits.

The 3D SQUID transmons also allow us to investigate if and how suspension affects their magnetic environments. In particular, many previous works have observed  $1/f$  flux noise experienced by several different

types of superconducting qubits<sup>8-10</sup>. It has been proposed that, similarly to dielectric loss, flux noise can be caused by defects in amorphous surface materials, such as silicon oxide<sup>19</sup>. However, typical measured flux noise levels in SQUIDs have been orders of magnitude higher than estimates based on known sources, and the origin of this important dephasing mechanism for superconducting qubits remains uncertain<sup>9,10,25</sup>.

In order to measure the noise power spectral density (PSD) of the qubits, we use the technique demonstrated in Bylander *et al.*<sup>25</sup>. We measure the response of the qubits to a collection of Carr-Purcell-Meiboom-Gill (CPMG) dynamical decoupling sequences with varying time delays and number of pulses to filter out noise at different frequencies. We can then use this in combination with the measured frequency-flux curves for the qubits to extract the PSD within a range of noise frequencies<sup>21,25</sup>. The results are shown in Figure 3d. The PSD's include data from two pairs of regular and suspended qubits measured in the same cavity on successive cooldowns. The data from the two pairs of qubits agree very well with each other, indicating that observed differences between the two types of qubits are not due to sample to sample variations. The flux noise for both qubits exhibits a clear power law dependence with an exponent of  $\alpha = 0.8 \pm 0.2$  for the suspended qubit and  $\alpha = 0.9 \pm 0.4$  for the regular qubit. We find that, while the PSD of both qubits is consistent with the range of previous measurements, the flux noise of the suspended qubits is higher than the regular qubits by a factor of of  $\sim 3$  in the frequency range measured. We also performed the same measurements at the zero-flux points of each qubit, and found that the PSD was essentially flat at the level of  $10^{-16}\ \Phi_0^2/\text{Hz}$ . This suggests that the measured noise in this frequency range is likely to be flux-related and not due to, for example, critical current fluctuations.

While one might expect that removing the substrate from underneath the SQUID loop would decrease the flux noise due to surface spins, our data indicates that the opposite effect occurs. It has been suggested that the dominant contributors to flux inside the SQUID loop are spins on the surface of the loop traces<sup>19</sup>. Therefore, removing the silicon surface inside and outside the loop may not have a large effect on the flux noise. On the other hand, DRIE also exposes the bottom surface of the aluminum loop, which forms a layer of amorphous  $\text{AlO}_x$  in air. Our observations are consistent with the new  $\text{AlO}_x$  layer having a higher concentration of spins than the aluminum-silicon interface, possibly because most of the  $\text{SiO}_x$  was removed by BOE prior to deposition. The observation that the flux noise increased by more than a factor of two after etching could suggest that the new  $\text{AlO}_x$  layer on the bottom surface contains more defects than the top surface. This might be the case given that the top oxide layer was grown in pure oxygen conditions inside the evaporator rather than through exposure to air<sup>26</sup>. We emphasize that while this explanation is consistent with our observations, further investigation would

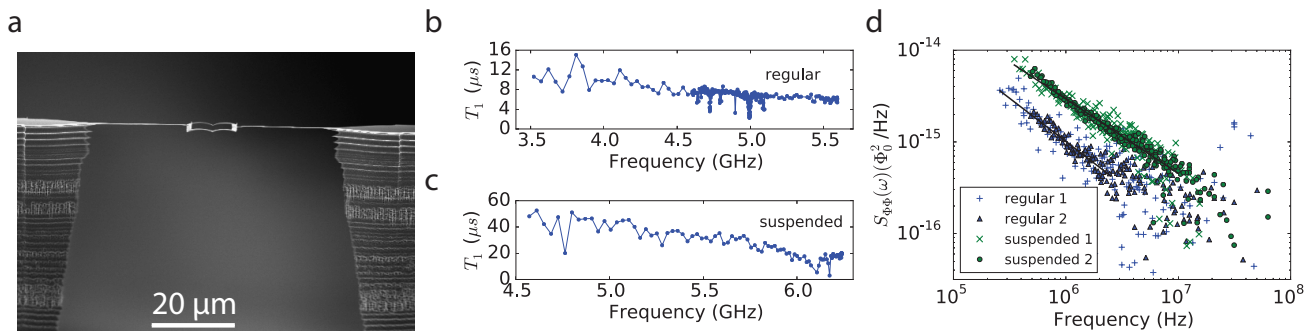


FIG. 3. **Flux tunable suspended qubits** (a) Side view SEM image of a suspended SQUID transmon. (b, c)  $T_1$  vs qubit frequency for regular (b) and suspended (c) qubits. See supplementary materials<sup>21</sup> for zoomed-in view of a low- $T_1$  feature in (b). (d) PSD of flux noise extracted from dynamical decoupling of regular and suspended qubits, each including data from two qubits. Solid lines are fits to the data. The extent of the lines indicate the frequency range in which the data was above the noise floor and therefore included in the fit.

be needed to elucidate the microscopic origins of additional flux noise in suspended qubits.

We have demonstrated that micromachining of silicon substrates is compatible with aluminum Josephson junction qubits. The process results in a reduction of the metal-substrate interface and an improvement of qubit  $T_1$ 's. Our results seem to suggest that we are approaching a regime where qubit decay is dominated by other mechanisms such as dielectric loss of the bulk silicon substrate. The loss tangent of “undoped” high-resistivity silicon is not very well known or understood, and is likely to be dependent on residual dopants and defects. We speculate that the DRIE technique described here, in combination with higher quality substrates, can result in qubits with even longer lifetimes. In addition, MS and bulk participation ratios can be further reduced by redesigning the qubit so that the DRIE process suspends larger areas of the device. We emphasize, however, that dielectric loss will eventually become dominated by another material. Even in the limit of a qubit floating in vacuum, there will be dielectric loss due to, for example, oxide on the surface of the metal. Beyond the reduction of dielectric loss, our measurements of flux noise with suspended SQUID transmons is another example of how qubit properties can be altered by changing the geometry of the substrate and the materials present in the environment. We expect that other potential loss mechanisms for cQED devices, such as quasiparticles and phonon coupling<sup>27,28</sup>, will also be affected. Therefore, our process provides a tool for understanding and improving the various aspects involved in the performance of superconducting qubits.

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# Supplemental Materials for "Suspending superconducting qubits by silicon micromachining"

## I. QUBIT DESIGNS AND FABRICATION PROCEDURES

Three types of 3D transmon qubit geometries were used to vary the surface participation in Figure 2 of the main text. They were similar to the designs used in Wang *et al.*<sup>4</sup>, and are shown in Figure S1. Design A, which had the lowest surface participations, was used to study the effects of DRIE etching.

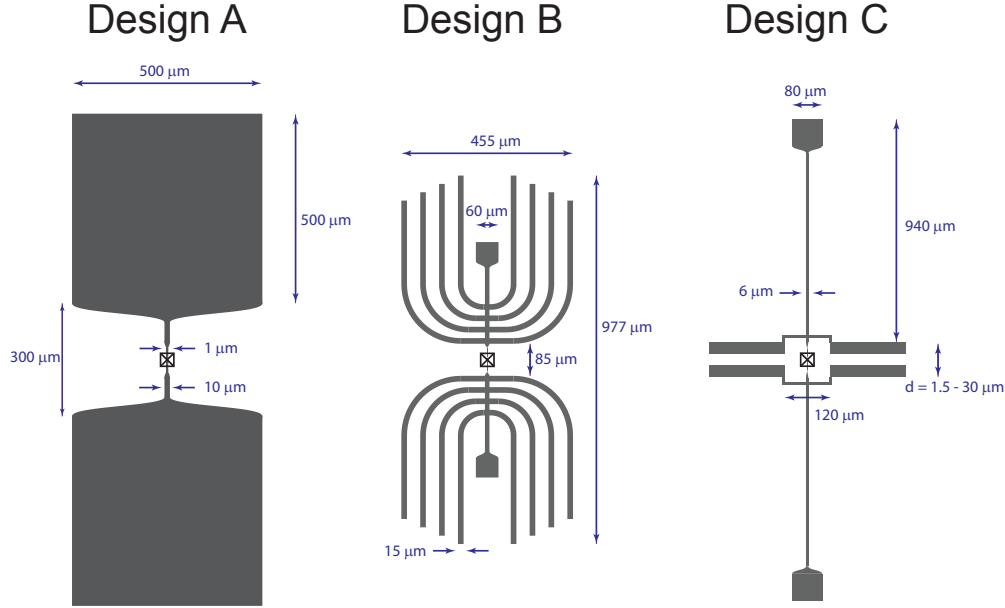


FIG. S1. **Transmon qubit geometries used in this study** The surface participations of Design C were varied by changing the distance  $d$  between the planar capacitor features.

Table S1 shows the various combinations of fabrication steps performed on Design A qubits and the resulting best  $T_1$ 's. Fabrication of all qubits was performed using the Dolan bridge technique on 300-500  $\mu\text{m}$  thick (100) high resistivity ( $\rho > 10^4 \Omega\text{cm}$ ) silicon wafers (Crystec and SiliconQuest). After cleaning in acetone and methanol, the wafer was spun with a bilayer of e-beam resist consisting of 500 nm of MMA (8.5) MAA EL 13 and 70 nm of 950K PMMA A3, then baked at 175  $^\circ\text{C}$ . Patterning of the qubit was done on a 100 kV VISTEC EBPG 5000+ e-beam writer, and the wafer was subsequently developed for 55 seconds in 1:3 MIBK:IPA followed by a 5 second rinse in IPA. For some of the devices, the developed wafer was then either etched in 10:1 BOE for 10 s or in an oxygen plasma asher (Glow Research AutoGlow) at 100 W for 10 s. We call this post-development step "clean 1" in Table S1. The wafer was then loaded into a Plassys e-beam evaporation system (MEB550S or UMS 300). In the case of BOE, the wafer was kept in a vacuum box during transport to the evaporator, which takes about five minutes. A bi-layer of aluminum (20 nm and 60 nm) was deposited using double-angle evaporation. In between the two layers, the junction barrier was grown by thermal oxidation using using a 85:15 Ar: $\text{O}_2$  mixture at 15 Torr for 12 minutes. Finally, the aluminum was capped with another oxide layer grown at 3 Torr for 10 minutes. After deposition, liftoff was performed in 90  $^\circ\text{C}$  NMP for several hours, then rinsed with acetone and methanol. Prior to dicing into individual chips with one qubit each, a layer of photoresist was spun on the wafer to protect the qubits. After dicing in an ADT 7100 dicer, the resist was removed by rinsing in solvent.

The diced chips were then optionally oxygen plasma ashed (OPA) at 100 W for 3 minutes (clean 2) and/or DRIE etched. The DRIE was done using the BOSCH process with alternating  $\text{SF}_6$  inductively coupled plasma (ICP) etch (10 s, 35 mTorr, 700 W) and  $\text{C}_4\text{F}_8$  ICP passivation (3s, 35 mTorr, 700 W) steps. The plasma was turned off for 1 minute after every 5 etch/passivation cycles to prevent overheating of the sample. By changing the ratio of the etch and passivation step times, we can control the amount of undercut and the orientation of the sidewalls. A larger ratio results in a larger undercut and a sidewall that slopes more inward with etch depth. Finally, the total number cycles controls the overall depth of the etch. We find that a 10s/3s etch/passivation cycle, resulting in a  $\sim 700$  nm undercut,

and a 60  $\mu\text{m}$  etch depth gives a significant modification of the participation ratios without jeopardizing the structural integrity of the devices.

After DRIE, some of the chips were processed with OPA again at 100 W for 3 minutes to remove any deposited polymer that might remain from the BOSCH process (clean 3).

TABLE S1. **Effect of cleaning procedures and etching on qubit  $T_1$ s.** Parameters and placement of the clean and DRIE steps in the fabrication procedure are described in the text. BOE: Buffered oxide etch. OPA: Oxygen plasma ashing.

Clean 1	Clean 2	DRIE	Clean 3	Max $T_1$ ( $\mu\text{s}$ )
None	None	None	None	4
BOE	None	None	None	6
BOE	None	Yes	None	63
BOE	None	Yes	OPA	59
BOE	OPA	None	None	7
BOE	OPA	Yes	OPA	50
OPA	OPA	None	OPA	23
OPA	OPA	Yes	OPA	44

## II. SIMULATIONS OF DIELECTRIC PARTICIPATION

Simulations for surface and bulk dielectric participation ratios were performed a method similar to that in Wang *et al.*<sup>4</sup>. For the suspended qubits, the geometries of the various interfaces were modified accordingly, as shown in Figure S2.

The DRIE suspension processes affects the substrate-air (SA) and metal-air (MA) interfaces in a qualitatively different way than the metal-substrate (MS) interface. While it reduces the MS participation by about a factor of 5, it *increases* the SA participation by a factor of 4.5 and the MA participation by a factor of 3, as shown in Table S2 and S3. As mentioned in the main text, the increase of these participation ratios could contribute to additional loss in the suspended qubits, which would explain why their  $T_1$ 's fall below the constant MS loss tangent line in Figure 2 of the main text. However, it is evident from Figure S3 that the unetched Design A qubits have shorter  $T_1$ 's than would be expected from a constant MS, SA, or MA loss tangent. Therefore, as proposed in the main text, an additional loss mechanism is needed to explain this discrepancy. The simplest model assumes an effect that is independent of surface participations, such as bulk dielectric loss.

TABLE S2. **Surface participation ratios for various qubits** The dimensions indicated for Design C are the gap sizes  $d$  for the planar capacitors, as shown in Figure S1.

Qubit	MS	SA	MA
Design A, suspended	1.25e-5	2.90e-4	5.74e-6
Design A, regular	6.16e-5	6.40e-5	1.90e-6
Design B,	1.39e-4	1.64e-4	1.45e-5
Design C, 30 $\mu\text{m}$	3.32e-4	3.83e-4	3.53e-5
Design C, 20 $\mu\text{m}$	3.96e-4	4.55e-4	4.22e-5
Design C, 10 $\mu\text{m}$	5.63e-4	6.49e-4	6.19e-5
Design C, 6 $\mu\text{m}$	7.64e-4	8.85e-4	8.74e-5
Design C, 3 $\mu\text{m}$	1.25e-3	1.46e-3	1.55e-4
Design C, 1.5 $\mu\text{m}$	2.16e-3	2.36e-3	3.16e-4

## III. RESONANT LOSS FEATURES

Both suspended and non-suspended flux tunable SQUID qubits exhibited dips in  $T_1$  at certain frequencies, consistent with resonant loss mechanisms usually attributed to TLS's in previous works<sup>5,24</sup>. They appear to be more prevalent

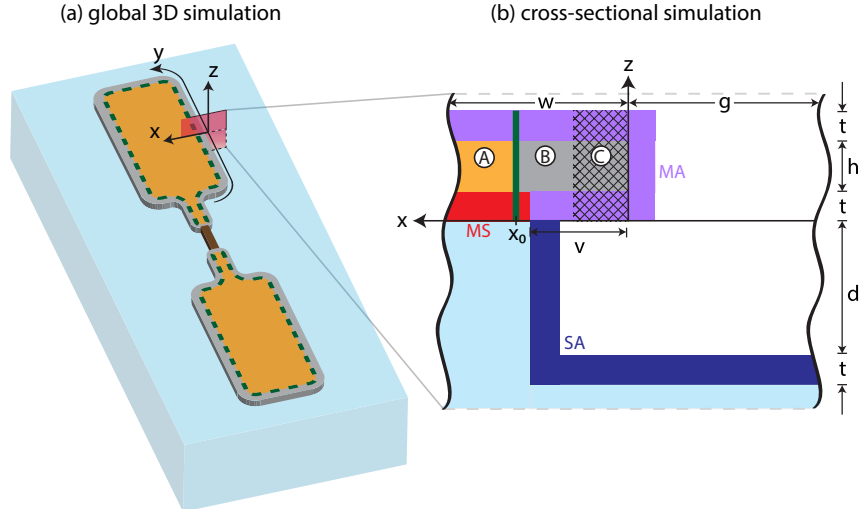


FIG. S2. **Simulation geometry.** (a) An isometric overview of the transmon pads on a silicon substrate (light blue). The leads near the junction, completely suspended in DRIE processed geometries, are shown in brown. The separation of the inner region (orange) and exterior region (gray) of the pads is indicated by a green dashed line. A slice taken on the  $xz$  plane is shaded in red. (b) The slice taken in (a) shows the etch profile, including the metal overhang (width  $v$ ) and deep substrate etch ( $\sim d$  deep). Interface surfaces are assumed to share a common thickness  $t$ , taken here to be 3 nm. The MS layer (red), which would normally extend to the edge of the metal, is reduced by the etch. The MA layer (purple) also includes the underside of any metal freshly exposed by the etch. The SA layer (dark blue) includes the sidewall surface of the remaining support substrate, increasing coverage significantly compared to unetched devices. The scalloped profile of the SA surface was approximated using a smooth plane. In accordance with the procedure in Wang *et al.*<sup>4</sup>, the perimeter region (gray) is divided into a cross-hatched region  $\textcircled{C}$ , which can fail to converge in the global simulation if  $v$  is small compared to  $x_0$ . The region  $\textcircled{B}$  is convergent in both simulations, and is used to bridge them in order to calculate the energy in the layers within region  $\textcircled{C}$ . The division between  $\textcircled{A}$  and  $\textcircled{B}$ , at  $x = x_0$ , separates the inner and exterior regions. All dimensions are not to scale.

in the non-suspended qubits, which exhibited several of such features of various widths. A detailed measurement of  $T_1$  versus frequency around one of these features is shown in S4.

#### IV. FLUX NOISE ANALYSIS

The power spectral densities (PSD) of the flux noise experienced by suspended and regular SQUID transmons were measured using dynamical decoupling techniques as described in Bylander *et al.*<sup>25</sup>. We briefly summarize the procedure here.

We applied a series of Carr-Purcell-Meiboom-Gill (CPMG) sequences<sup>29</sup>, given by

$$\left(\frac{\pi}{2}\right)_x - \left[\frac{\tau}{2N} - \pi_y - \frac{\tau}{2N}\right]^N - \left(\frac{\pi}{2}\right)_x \quad (\text{S1})$$

followed by dispersive measurement of the qubit state. The qubits were tuned to some flux point near  $\Phi_0/4$  where the  $T_1$  was relatively long. In our case, the measured signal is given by

$$\chi_N(\tau) = A_0 + A \left(\frac{\partial\omega_q}{\partial\Phi}\right)^2 \tau^2 \int_0^\infty d\omega S_{\Phi\Phi}(\omega) g_N(\omega, \tau) \quad (\text{S2})$$

Where  $\omega_q$  is the qubit frequency,  $A_0$  and  $A$  are an overall offset and scaling determined by the qubit readout parameters, and  $S_{\Phi\Phi}(\omega)$  is the PSD of the flux noise. By varying the length of the total sequence  $\tau$  and the number of echo pulses  $N$ , we can vary the center frequency and bandwidth of the filter function  $g_N(\omega, \tau)$  that makes the dynamical decoupling sequence sensitive to a particular part of the noise spectrum<sup>30,31</sup>. The expression for  $g_N(\omega, \tau)$  for the CPMG sequence can be found in the supplementary materials for Bylander *et al.*<sup>25</sup>.

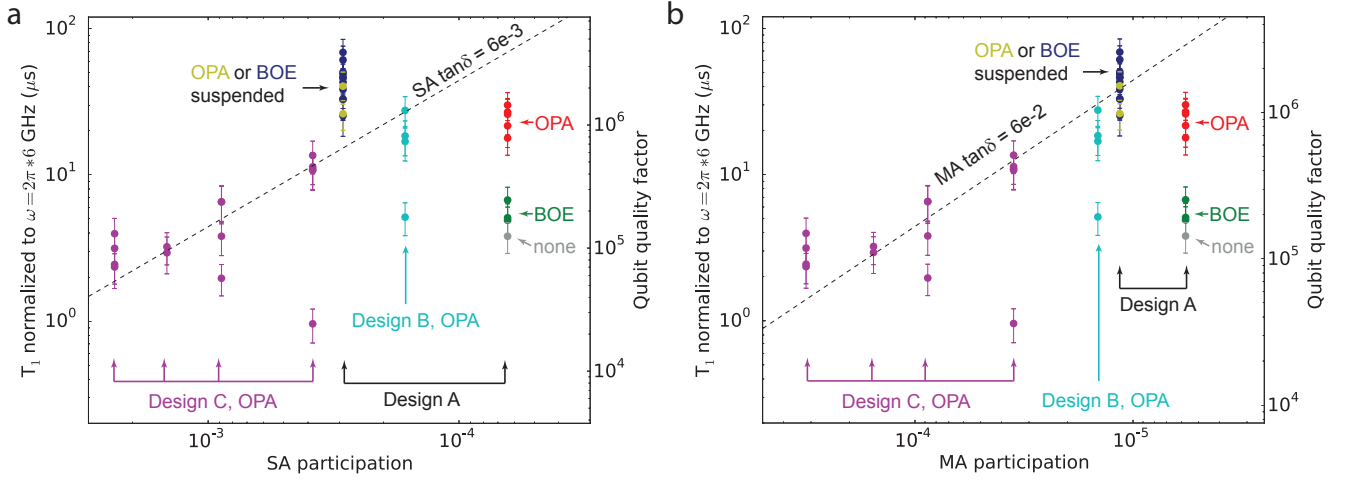


FIG. S3. **Lifetime of silicon transmons vs. SA (a) and MA (b) participation ratios.** Dashed lines are guides to the eye corresponding to the indicated dielectric loss tangents.

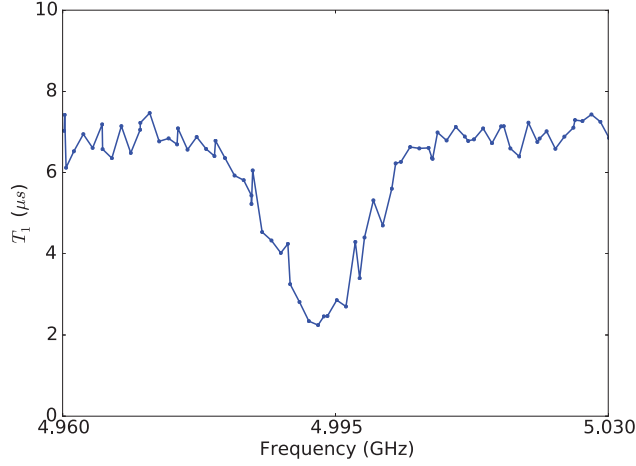


FIG. S4. **Resonant loss feature in non-suspended SQUID qubit** Zoom-in on one of the resonant features in Figure 3b of the main text.

Our goal is to invert equation S2 in order to determine  $S_{\Phi\Phi}(\omega)$  from the raw data. Each set of raw data consists of varying  $\tau$  for a fix number of echo pulses, an example of which is shown in Figure S5a. We then fit the data to a functional form

$$A_0 + Ae^{-\frac{(\tau-\tau_0)^2}{2T_2^2}} e^{-\frac{\tau-\tau_0}{T_1}}, \quad (\text{S3})$$

which takes into account the independently measured  $T_1$  decay of the qubit and assumes a particular functional form for the dephasing, which of course depends on the flux noise PSD that we would like to determine. Therefore, the fit is only used to extract  $A_0$ ,  $A$ , and  $T_2$ , which are used to normalize the raw data and determine the range of  $\tau$  for which the data is above the noise floor.

Next, we simplify the problem by assuming that  $g_N(\omega, \tau)$  is sharply peaked and replace it with a rectangular filter function with the same height and width. This becomes a better approximation for larger  $N$  and  $\tau$ . Using this simplified filter function, we can calculate the power spectral density of the *frequency* noise. An example is shown in Figure S5b after combining datasets with different  $N$ 's for one of the suspended qubits. Note that each data point in the raw data corresponds to one data point in the PSD. Finally, to convert this into flux noise, we determine  $\partial\omega_q/\partial\Phi$  by measuring the flux tuning spectrum of the qubits.



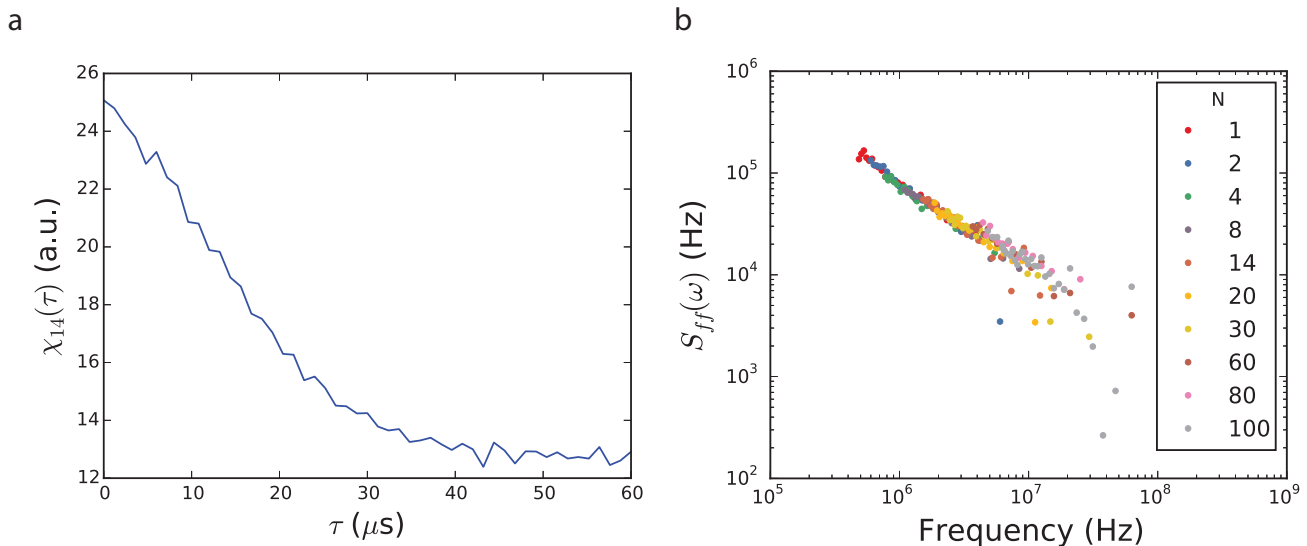


FIG. S5. **Determination of flux noise PSD** (a) Raw CPMG data with  $N = 14$ . (b) PSD of frequency noise for a suspended qubit including data for all different  $N$ 's.

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